CIRCUIT DESIGNER'S NOTEBOOK

Capacitors in Coupling and DC Blocking Applications

Capacitors used in coupling and dc blocking applications serve to couple RF energy from one part of a circuit to another and are implemented as series elements. Proper selection of coupling capacitors insures the maximum transfer of RF energy. All capacitors will block dc by definition; however, considerations for satisfying the requirements of a coupling application depend on various frequency-dependent parameters that must be taken into account beforehand.

Figure 1 illustrates two RF amplifier stages operating in a 50-ohm network interconnected by coupling capacitor C_0. Table 1 outlines several device options for achieving interstage coupling at various wireless frequencies. Electrical parameters such as series resonance, impedance, insertion loss, and equivalent series resistance must be evaluated in order to achieve an optimal coupling solution.

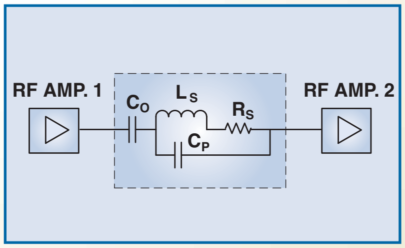

Figure 1: Interstage coupling block diagram

Note: Coupling capacitor C_0 in Figure 1 is represented with its equivalent series resistance (ESR) denoted as R_S, equivalent series inductance (ESL) denoted as L_S and parasitic parallel capacitance C_P, associated with the parallel resonant frequency (F_{PR}).

Frequency (MHz)	Device Options	FSR (MHz)	Insertion Loss S21 (dB)	ESR (ohms)	Package Size
900	100A101 – 100 pF	1000	< 0.1	0.072	55 mil x 55 mil
	600S101 – 100 pF	1340	< 0.1	0.070	0603
1900	100A270 – 27 pF	1870	< 0.1	0.161	55 mil x 55 mil
	600S560 – 56 pF	1890	< 0.1	0.085	0603
2400	100A160 – 16 pF	2410	< 0.1	0.218	55 mil x 55 mil
	600S390 – 39 pF	2340	< 0.1	0.140	0603

Table 1: Examples of coupling capacitors & associated parameters

A capacitor's series resonant frequency (F_{SR}) also referred to as self-resonance, occurs at

$$F_{SR} = \frac{1}{2\Pi\sqrt{L_S C_O}}$$

At this frequency the capacitor's net reactance is zero and the impedance is equal to the ESR. As shown in Table 1, an ATC100A101, (100 pF) porcelain capacitor has an F_{SR} of 1000 MHz with a corresponding ESR of 0.072 ohms. At this frequency the capacitor will provide its lowest impedance path required for optimal coupling. In contrast the impedance of a capacitor at its parallel resonant frequency (F_{PR}) can be precipitously high. By assessing the magnitude of S21 vs. frequency for a given capacitor, excessive losses associated with F_{PR} at the operating frequency can be readily observed. In coupling applications a capacitor's F_{SR} can usually be exceeded without posing a problem as long as the net impedance remains low.

Net Impedance

The magnitude of a capacitor's impedance is equal to

$$\sqrt{(ESR)^2 + (X_L - X_C)^2}$$

As seen by this relationship a capacitor's impedance is significantly influenced by its net reactance (X_C - X_L). It is important to know the magnitude of the impedance throughout the desired passband. A properly selected coupling capacitor will exhibit suitably low impedance at these frequencies.

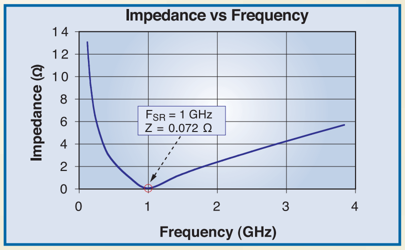

Figure 2: Impedance vs. Frequency for ATC100A101 (100pF)

As seen in Figure 2 the net impedance below F_{SR} is capacitive and is dominated by $1/\omega C$ yielding a hyperbolic curve for frequencies less than F_{SR}. Conversely, the net impedance above F_{SR} is inductive and is dominated by ωL yielding a linear line segment for frequencies greater than F_{SR}.

Insertion Loss (S21)

One of the fundamental considerations for all coupling applications is the capacitor's insertion loss at the operating frequency. By evaluating the magnitude of S21 the designer can readily determine whether or not the subject capacitor is suitable. It is especially important to look for the presence of one or more parallel resonances falling within the operating passband. These resonances will generally show up as distinct attenuation notches at their frequencies of occurrence. If a parallel resonance does fall within the operating passband it will be necessary to evaluate its depth in order to determine whether or not the loss is acceptable. In many instances the magnitude of S21 for a given capacitor may be excessive, rendering it unusable for the application. An insertion loss of several tenths of a dB is generally an acceptable criterion for most coupling applications. Losses that exceed several tenths of a dB within the passband could easily compromise the end performance of a circuit design. Therefore the decision is ultimately left up to the discretion of the designer to determine whether or not these losses are acceptable for a particular design requirement.

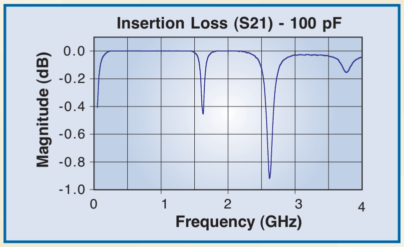

Figure 3: Insertion loss vs. Frequency for ATC100A101, 100 pF chip capacitor in flat mount orientation

Figure 3 illustrates the insertion loss characteristic of an ATC100A101 (100pF) capacitor. The sample was measured in a series through configuration from 50 MHz to 4 GHz with the capacitor's electrodes parallel to the substrate, i.e. flat mount orientation. As seen in figure 3 the capacitor's insertion loss is less than 0.1 dB between 200 MHz to 1.5 GHz. By edge mounting the capacitor, i.e. electrodes perpendicular to the substrate, the first parallel resonant notch at 1.6 GHz will be suppressed. As a result the usable frequency range will be extended to approximately 2.4 GHz. In this orientation the same capacitor can be used to include all of the wireless frequencies in a broadband coupling application.

ESR and Q

A capacitor's quality factor (Q) is numerically equal to the ratio of its net reactance ($X_C - X_L$) to its equivalent series resistance

$$Q = \frac{|X_C - X_L|}{ESR}$$

From this expression it can be seen that the capacitor's Q varies inversely to its ESR and directly with the net reactance. A capacitor's ESR should be known at all frequencies within the passband, especially at frequencies above the capacitor's series resonant frequency. At the frequency where the electrode thickness is at least one skin depth the ESR will increase as the $\sqrt{f}$. Accordingly, the ESR will increase in this fashion for increasing frequencies and may become the dominant loss factor. As previously mentioned an attenuation notch will occur at the capacitor's F_{PR}, the depth of which is inversely proportional to the ESR. Therefore the capacitor's ESR will largely determine the depth of the attenuation notch at the parallel resonant frequency.

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