ATC // AVX THIN FILM TECHNOLOGIES

Engineered Thin Film Solutions

THE ENGINEERS' CHOICE®

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ATC // AVX Thin Film Technologies

Engineered Thin Film Solutions

ATC // AVX is pleased to introduce the combined resources of ATC's Jacksonville, Florida and AVX's Myrtle Beach, South Carolina Thin Film product groups. This allows us to offer a wide range of custom hybrid circuits along with thin film resistors, capacitors, inductors, as well as lumped element and distributed filters, integrated passives, modules, heat sinks, and other unique thin film microelectronic solutions.

Myrtle Beach Thin Film Products

AVX Thin Film operations, located in Myrtle Beach, SC, offers an array of thin film passives including networked resistors, capacitors, inductors, along with integrated passive LC and RC filters and modules. Six inch (150 mm) wafer technology offers the designer build-to-print or custom designs based on 3D HFSS modeling from 500 MHz to 40 GHz. These products will meet the most demanding requirements of circuit miniaturizations, tolerance and signal integrity applications that involve a wide frequency spectrum from MHz to GHz.

Design, Fabrication, Assembly, and RF Testing Services

Jacksonville Thin Film Products

Since 1993, ATC Thin Film Products, located in Jacksonville, FL, has been supplying a broad spectrum of high reliability metalized hybrid circuits. Designers can select from a wide variety of substrate materials, as well as vias, crossovers and bridges. Whether built to print or designed to a performance specification, the experienced engineering staff is available to assist in optimizing your product. In addition, two-sided assembly and RF testing to 40 GHz are value-added services. AS-9100 certification ensures conformance with existing military and aerospace requirements.

ATC // AVX Thin Film Technologies, Myrtle Beach, South Carolina

Combined Capabilities

- Design: Modeling (HFSS), simulation (Genesys) and CAD (Tanner)
- Substrates: 1 inch square to 6 inch round (150 mm) wafers
- Typical materials: Alumina, Aluminum Nitride, Beryllium Oxide, Silicon, (N, P, and N+), Quartz, Glass, Glass-Ceramic, Sapphire, Ferrites and Titanates
- Metalizations:
  Sputtered: Al, Au, Cr, Cu, Ni(V), Pt, TaN, Ti and TiW
  Plated: Electrolytic Cu, Ni, Au; Electroless Cu, Au
- Resistors: High Ohmic SiCr and TaN resistors in laser trimmable designs
- Capacitors: Si02, SiON and BCB dielectrics in laser trimmable designs

ATC // AVX Thin Film Technologies - Jacksonville, Florida

AMERICAN TECHNICAL CERAMICS

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- Inductors: Multilevel and multiturn copper and gold inductors
- Routing: True Air Bridges and Dielectric Crossovers
- Passivation Materials: SiON, Si_3N_4, BCB and polyimide
- Vias: Sputtered, enhanced plated, filled and castellations
- I/Os: BGA, LGA, edge wrap, through via and wire or ribbon bond
- Machining:
  - CO2 cutting, drilling, and scribing
  - Diamond-saw dicing
  - Back grinding and polishing
- Assembly:
  - High precision 0201 or larger pick and place
  - Attachment via wire or ribbon bonding, BGA, LGA or surface mount reflow
  - Encapsulation
- Testing:
  - MIL-STD-105D level II sampling
  - MIL-STD-883 100% visual inspection
  - Capacitance, insulation resistance and resistivity
  - RF testing to 40 GHz
  - RF and Microwave filters
  - Precision resistors
  - MOS capacitors
  - Circulators, Splitters
  - Specialized modules
- Medical and Instrumentation:
  - Precision resistor networks and arrays
  - In-circuit trimmed designs
  - Telemetry filters
  - Miniature circuits and assemblies
- Broadband infrastructure:
  - Laser diode mounts and heat sinks
  - Optoelectronic converters
  - RF and DC fan-outs
- Instrumentation:
  - Ultra-precision reference capacitors and resistors
- Solar:
  - Interposers and heat sinks

Primary Markets and Applications

- Military, Aerospace and Space:

Typical Substrate Properties

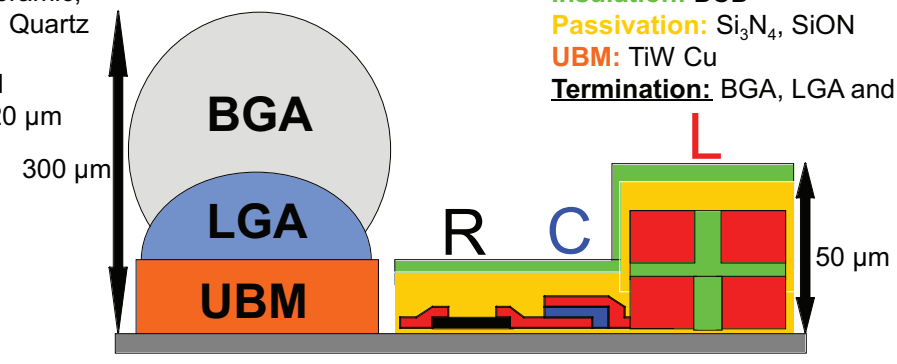
Properties Nominal	Al_2O_3 99.6%	Al_2O_3 96.0%	Fused Silica	BeO 99.5%	AIN	Glass Boro-silicate	Glass Ceramic	P-Silicon Boron Doped	N^{++}-Silicon Arsenic Doped	FZ-Silicon Arsenic Doped
Thickness Range (mil)	4-50	10-50	4-25	10-60	10-60	20	20	2-25	4-25	4-25
As Fired (Surface finish)	3µ''	No	No	6µ''	No	10 Å	N/A			
Lapped (Surfance finish) µ''	<20	No	No	<20	<20	N/A				
Polished (Surfance finish) µ''	<2	<4	<1	<3	<3	<.04	<0.6	<.04		
Dielectric Constant @ 10 GHz	9.8	9.6	3.8	6.6	8.7	5.1	N/A			
Loss Tangent @ 10 GHz	0.0002	0.0002	0.0001	0.0003	0.001	0.003	N/A			
CTE (PPM/°C)	6.7	8.2	0.5	7.5	4.5	3.2	11.5	2.6		
Thermal Conductivity (W/mK)	25.5	24.7	1.38	280	170	1.16	2.7	150		
Volume Resistivity (ohm-cm)	10^{14}	10^{14}	10^{14}	10^{14}	10^{13}	10^{13}	10^{13}	15	0.002	10^{4}
Dielectric Strength (KV/mm)	8.7	8.3	100	14	>10	N/A				

Sputtered and Electroplated Materials

Materials	Sputtered	Comment
Al	150-40000 Å	AlSi (<1%) and AlCu (2%) available, Typical 2000 – 15000
Au	1000-65000 Å	Typical 3000 – 10000
Cr	150-5000 Å	Typical 600
Cu	2000-65000 Å	N/A
LSCO	300-1200 Å	Typical 600
Ni(V)	500-10000 Å	N/A
Pt	1000-4000 Å	Typical 2500
TaN	300-1500 Å	Barrier Layer
Ti	500-5000 Å	Typical 600
TiW	300-1500 Å	Typical 500
Plated Material	**Electrolytic µm and (µin)**	**Electroless µm and (µin)**
Au	0.5 – 50 (20-2000)	1-10 (40-400)
Cu	5 – 150 (200-6000)	2-4 (80-160)
Ni	1.25 – 5 (50-200)	N/A

Wafer Construction Overview

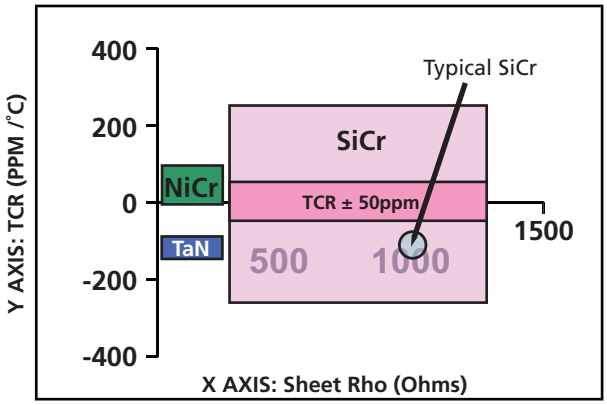
Substrates and Materials:
Wafer Substrates: Silicon, Ceramic, Glass and Quartz
Dielectrics "C": NPO
Resistors "R": SiCr and TaN
Conductor "L": Cu 1µm to 20 µm



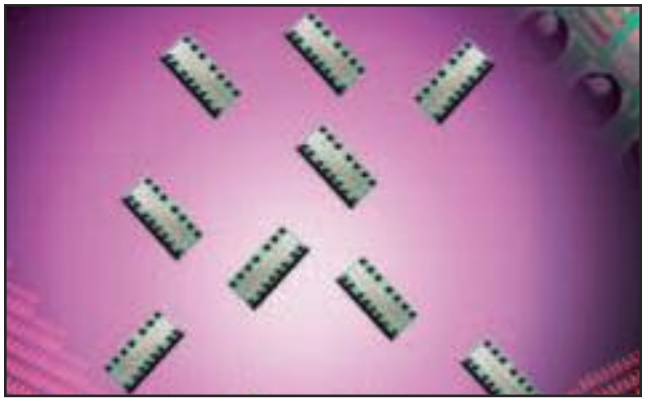
Passivation and I/O:
Insulation: BCB
Passivation: Si_3N_4, SiON
UBM: TiW Cu
Termination: BGA, LGA and WB

Resistor Technology

Thin Film Resistors	SiCr	TaN	NiCr
Process	High Ohmic, High Voltage, Ultra-stable	High process temperature (no diffusion); Resistance to harsh environment	Low TCR
Typical Sheet Resistivity (ohm/sq)	300-1300	10-200	5-200
TCR (ppm/°C -25 to 125°C))	±50; 0 to -150	-100 to -150	0 to 100
Stability (Change after 1000 hours @ 125°C)	0.2%	0.2%	0.2%
Maximum Stabilization Temperature (°C)	500	450	350
Recommended Device Environment	Ambient Atmosphere	Ambient Atmosphere	Ambient with Passivation or Inert Atmosphere
Maximum Device Processing Temperature	Up to 1 hr. @ 400 °C	Up to 1/2 hr. @ 350 °C	Up to 1/2 hr. @ 260 °C
Tolerance (the greater of)	0.05% or 0.1 Ω	0.05% or 0.1 Ω	0.05% or 0.1 Ω



Resistor Materials



Precision Resistors

Capacitor Materials

Material	SiON	SiO_2	BCB	PI
pF/mm² Typical	55	35	25	30
Range	1-500 pF	1-500 pF	1-50 pF	0.5-10 pF
Trimmable	Yes	No	Yes	No
Tolerance; *NOTE: value dependent*	≥ 0.5%; or ≥ 0.05 pF	≥ 0.5%; or ≥ 0.05 pF	≥ 0.5%; or ≥ 0.05 pF	20%
Stability	±60 ppm/°C	±30 ppm/°C	±42 ppm/°C	±100 ppm/°C
Rated Voltage	≤ 100	≤ 100	≤ 25	≤ 25
BDV (v/µm)	600	1000	300	200
DF	≤ 0.1%	≤ 0.1%	≤ 0.1%	≤ 0.2%
Performance	K 5.8; TCC 60	K 4.0; TCC 30	K 2.7; TCC 42	K 3.3; TCC

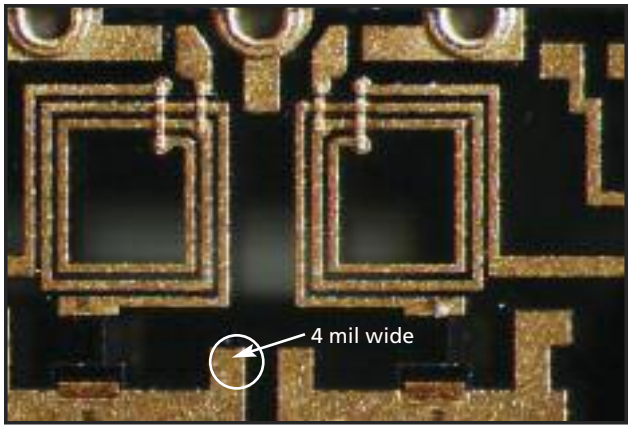
Precision Capacitors

Multi-target Sputter System

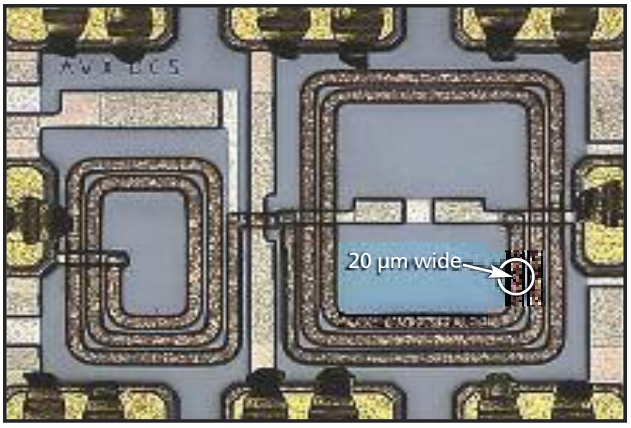
Inductors

Typical values range from 0.1 - 45 nH. The coil material consists of patterned plated copper or gold on a sputtered seed layer. The preferred substrates for hybrid assembly construction are supplied either polished or as-fired. Typical dimensions for hybrid substrate designs (in micrometers) are: 25 µm wide, 20 µm spacing at < 5 µm thick. 50 µm wide, 46 µm spacing at < 10 µm. thick, 125 µm wide, 100 µm spacing, 12.5 – 75 µm thick. See design summary below:

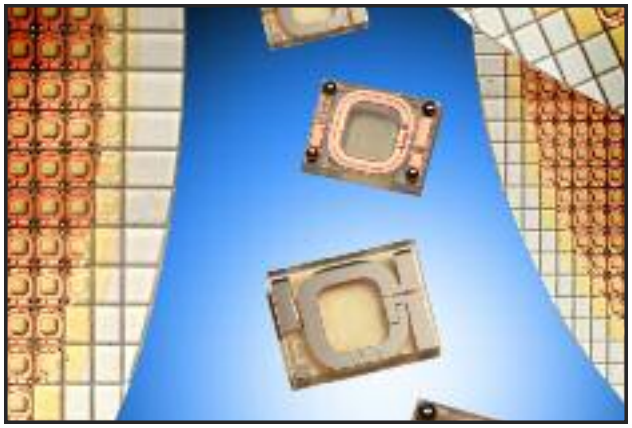
Construction Platform	Width (µm)	Spacing (µm)	Height (µm)
Hybrid	25	20	5
	50	46	> 10
	125	100	75
Wafer	> 10	> 10	Max 20*
*BCB Dielectric Separator layers 5-10 µm			



Hybrid Inductor



Wafer Inductor



Precision Inductors

Inspection

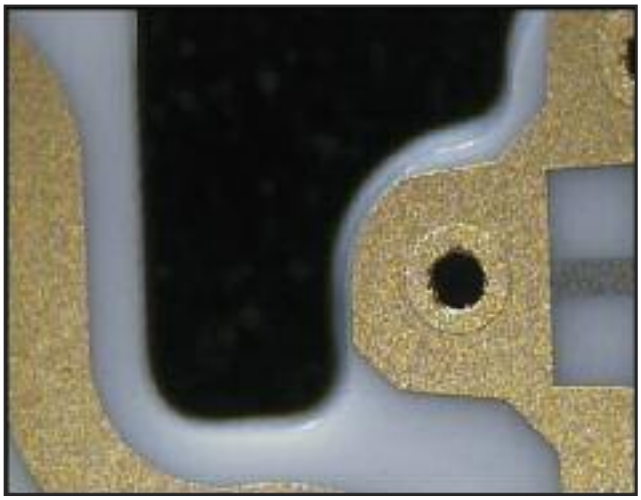
Typical Metalizations

Typical Hybrid Metalizations	Application	Attachment Method	Metalization/ Resistor Layers	Typical Value
1. TaN –TiW – Ni* – Au	RF/Microwave circuits: attenuators, loads and DC biasing networks. Hybrids with resistors and spiral inductors. End products: Power supplies, couplers, splitters, filters, amplifiers, SAW devices, laser diode mounts and others.	Pb/In, Au/Sn, Au/Ge – Eutectic Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å NiV 1000 to 2000 Å Au 20 to 300 µin	50 500 1500 150
2. TiW – Ni* – Au	Same as 1. – without resistors	Pb/In, Au/Sn, Au/Ge – Eutectic Epoxy Wire Bonding	TiW 300 to 1000 Å NiV 1000 to 2000 Å Au 20 to 300 µin	500 1500 150
3. TaN –TiW – Au – Ni – Au	Same as 1. – When repeated soldering is required for repairs	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å Au 20 to 300 µin Ni 50 to 150 µin Au 20 to 200 µin	50 500 20 min. 50 min. 150
4. TiW – Cu – Ni* – Au	High Power/Low Loss RF and Power Supply	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TiW 300 to 1000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	500 500 50 min. 150 min.
5. TiW – Au – Cu – Ni* – Au	High Power/Low Loss RF and Power Supply	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TiW 300 to 1000 Å Au 3000 to 5000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	500 3000 min. 500 50 min. 150 min.
6. TaN – TiW – Au Cu – Ni* – Au	High Power/Low Loss RF and Power Supply with Resistors	Pb/Sn, Au/Sn soldering Epoxy Wire Bonding	TaN 10 to 200 ohms/sq. TiW 300 to 1000 Å Au 3000 to 5000 Å Cu 200 to 2000 µin Ni 50 to 150 µin Au 20 to 200 µin	50 500 3000 min. 500 35 min. 150 min.

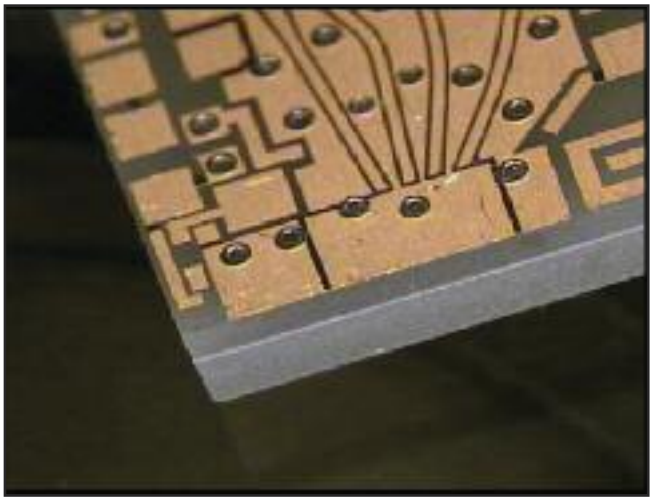
* Optional
Other metalizations available upon request.

Typical Hybrid Circuit Features

Circuit Feature	Specifications
Conductors:	Lines and spaces width ≥ .0005 inches
Resistors:	Tolerances ≥ 0.1%
Via Holes:	Conventional or Enhanced Vias®
Air Bridges:	Over Lange Coupler - To eliminate need for wire bonding
Crossovers:	With Polyimide over conductor lines
Wraparounds:	Edge patterning
Solder Dam:	Polyimide, Ni Oxide and others



Enhanced Via® (Filled Vias Available)

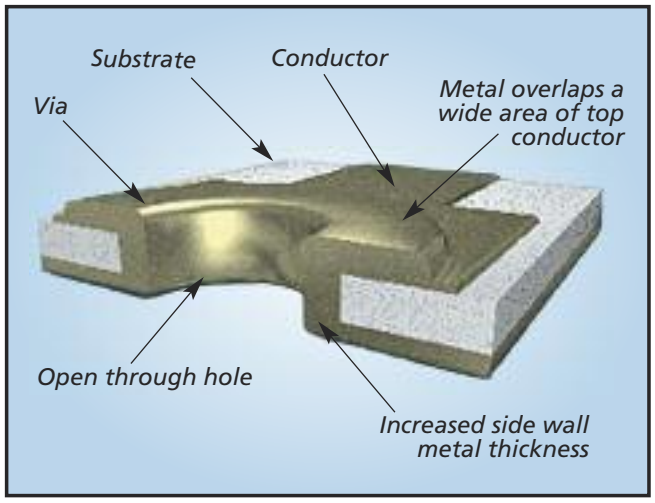


Ni Oxide Solder Dam Stop

Enhanced Vias®

Designed for Improved Performance:

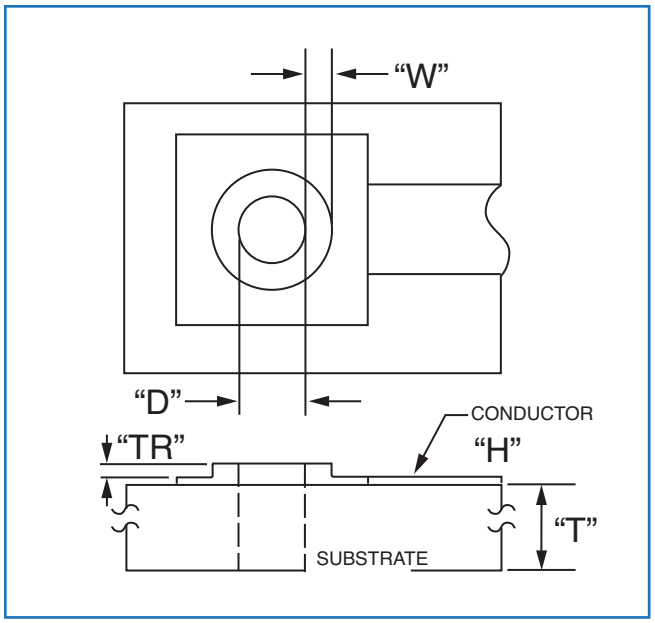
- Low contact resistance due to the increased metal thickness
- Uniform metallic connection to top and bottom surfaces ensures highest reliability and minimum contact resistance
- Increased overlap area improves robustness
- Pure plated Cu Au for epoxy and eutectic die-bond attachments
- Optional Ni barrier for solder attachments
- No ceramic filler materials
- Minimal occurrence of closed voids
- No entrapment of liquids and gases
- Through hole provides ability to visually inspect via after mounting to carrier
- Via plugging options available to prevent epoxy or solder wicking



Enhanced Via®

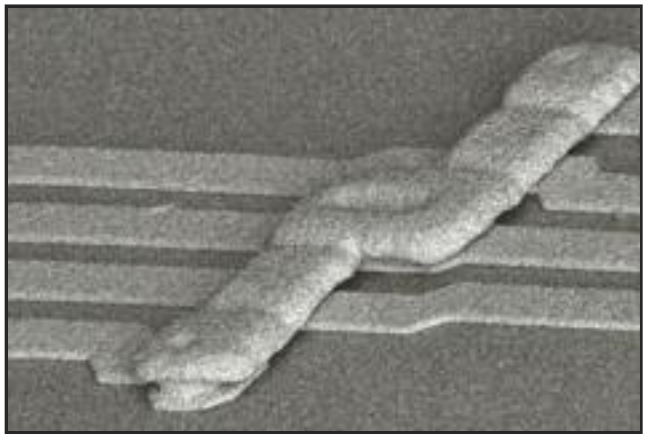
Design Guidelines for Enhanced Vias®

Parameter	Symbol	Limits/ Recommendations
Hole diameter	D	Minimum: 0.6 X T Nominal: >=1 X T
Rim width	W	Minimum: 0.002" Nominal: 0.005"– 0.025"
Rim thickness	TR	per request
Nominal DC Resistivity (mΩ) (T&D in mils, TR&H in µ")	$\frac{318 \times T}{D \times (TR+H)}$	



Air Bridges

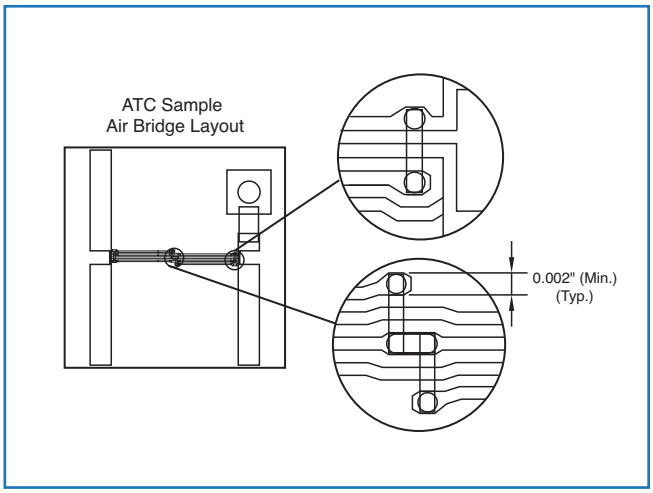
- Reliable bridging for 'too-small-to-wire' geometries
- Improved performance at high frequencies compared to wire-bonded bridges



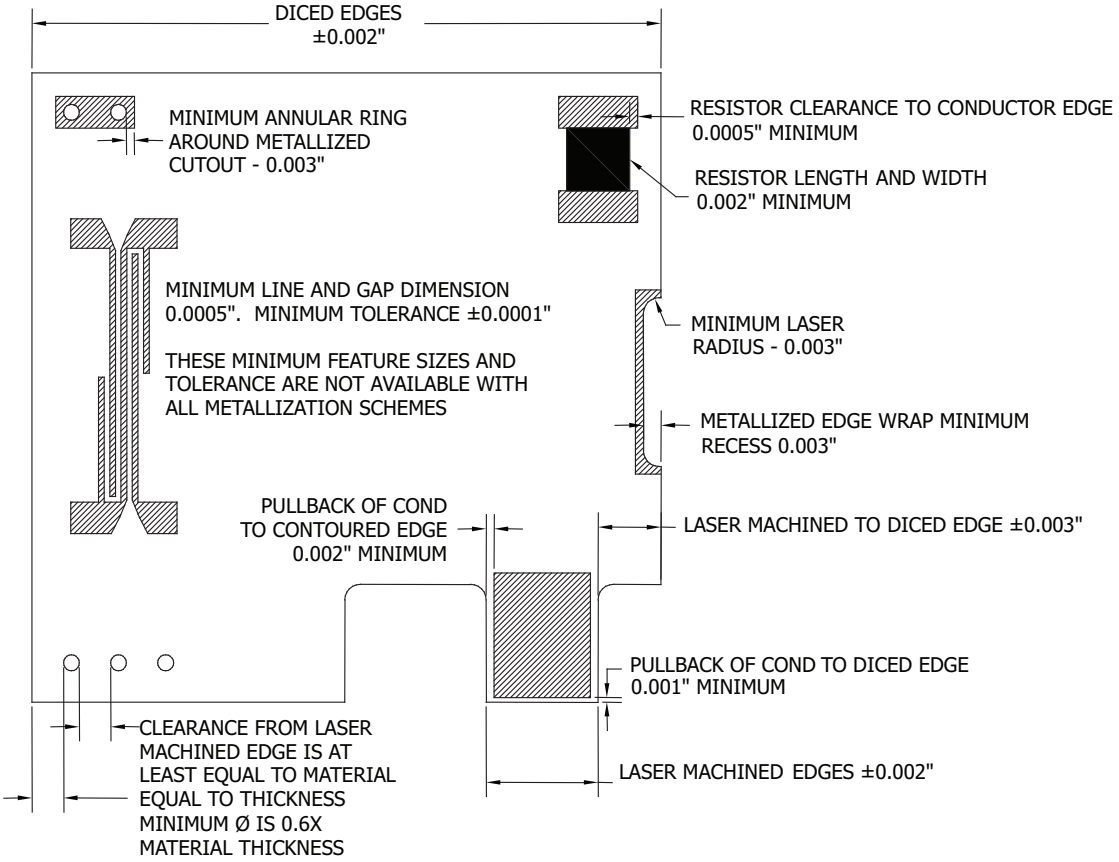
Air Bridge

Design Guidelines for Air Bridges

Parameter	Limits/Recommendations
Minimum gap between lines	0.5 mil (0.0005")
Minimum line width	0.5 mil (0.0005")
Minimum pillar's base diameter	2.0 mil (0.002")
Minimum pillar diameter	1.3 mil (0.0013")
Minimum bridge width	1.3 mil (0.0013")
Dielectric	Air (polyimide optional)



Hybrid Circuit Design Guidelines



LASER MACHINED CUTOUTS AND VIAS HAVE A TAPER EQUAL APPROXIMATELY TO 10% OF THE MATERIAL THICKNESS PER SIDE.

DIMENSIONS STATED ON THE SPECIFICATION ARE MACHINED TO MEET TOLERANCE ON THE SIDE OF THE CERAMIC WITH THE MAXIMUM MATERIAL CONDITION.

METALLIZED CUTOUTS ARE TO MEET THE SPECIFIED DIMENSIONS BEFORE METALLIZING UNLESS OTHERWISE SPECIFIED.

THIS IS PROVIDED AS A BASIC GUIDELINE. THIS DRAWING DOES NOT SHOW ALL FEATURES THAT ATC CAN PROVIDE.

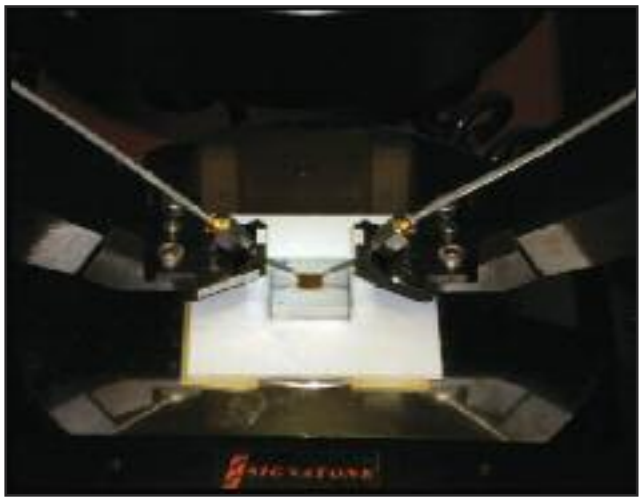
CONSULT WITH THE FACTORY CONCERNING FEATURES THAT ARE NOT INCLUDED ON THE DRAWING OR FOR REQUIREMENTS THAT VIOLATE THE GUIDELINES.

General Design Guidelines

		Hybrid (Inches)	Wafer (Micrometers)
Conductors	Minimum Line Width / Minimum Space Width	.0005	10
	Line Width Tolerance	.0002 Standard .0001 Select	±3
	Space Tolerance	.0002 Standard .0001 Select	±3
	Minimum Pad Size Around Via (D = hole diameter)	.006 + D	±10
Resistors	Minimum Tolerance	greater of 0.1% or 0.1 Ω	.01%
	Minimum Spacing Between Resistors	.002	4
	Minimum Length and / or Width	.002	4
	Pre Trim Designed Value	–20%	-20%
	Nominal Sheet Resistance (ohms / □) Preferred Sheet Resistance (ohms / □)	10 – 200 50 or 100	30-1500 (ohms / □)
Terminations	Minimum Pad Size (Wire Bond)	.003 x .003	75 x 75
Metalized Holes (VIA's)	Minimum Aspect Ratio (Hole diameter: Substrate thickness)	0.6:1	N/A
	Minimum Tolerance	.002	
	Minimum Distance from Hole Circumference To Edge (T = substrate thickness) or adjacent hole circumference	T	
	Minimum True Center Tolerance	.001	
Substrates	Minimum Thickness Tolerance	.0005	10
	Minimum Length / Width Tolerance	.001	N/A
	Surface Finish (Microinch – CLA not available in all materials)	.2 – 10	.001
	Minimum Camber (Polished only) Typical Camber – Polished Typical Camber – As Fired	.0002 / inch .0005 / inch .002 / inch	10 across 150 millimeters
Data Format	DXF, DWG, GDSII, Gerber (Consult Factory For Other Formats)	All formats	DXF, GDS II
	Closed Polylines (0 Width)	Traces	
	Minimum Resistor On Conductor Overlap	.002	10

RF Testing Capability

ATC // AVX RF test capabilities include full two (2) and four (4) port test measurements using a vector network analyzer. Compensation up to the device under test (DUT) is typically performed with a custom calibration (short-open-load- through - SOLT) method to acheive the most accurate measurements possible. When necessary, other methodologies are employed. In addition, specialized test structures are designed and fabricated in-house for specific requirements of the DUT. The typical frequency measurement range is from 50 MHz to 20 GHz with optional testing capability to 40 GHz. An automated in-line data analysis system enables a quick pass-fail sorting process to a frequency-defined template, or provides serialized complete S-Parameter data for the customer.

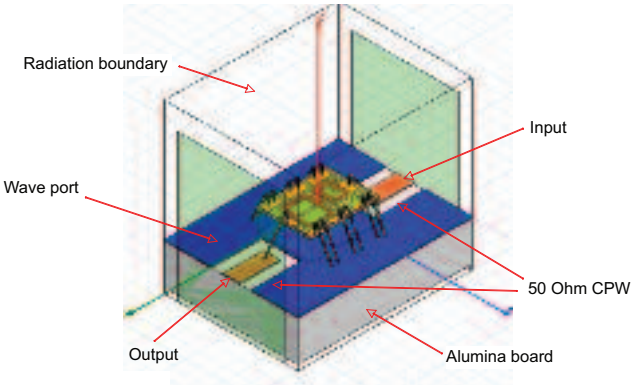


Modeling

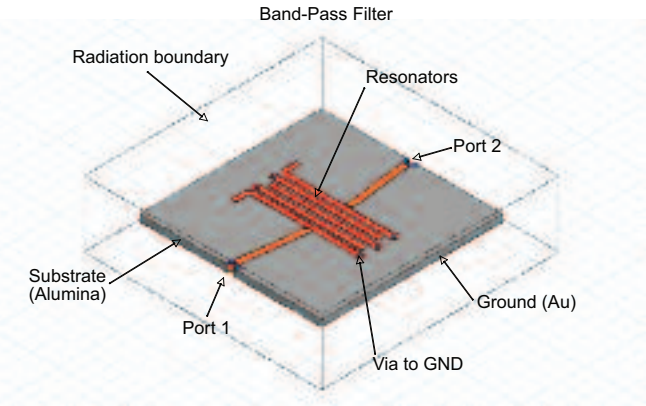
ATC // AVX models utilize Ansoft HFSS full 3D geometry software. This method uses finite element analysis of the models using tetrahedrons to obtain a 3D design. The combination of the 3D design and selection of appropriate dielectric materials and metalization is critical to the final design. The close correlation between the design, models and materials, offers the advantage of virtual processing. All designs are validated with measurements during the fabrication build process.

Complete Radiation Environmental Simulation

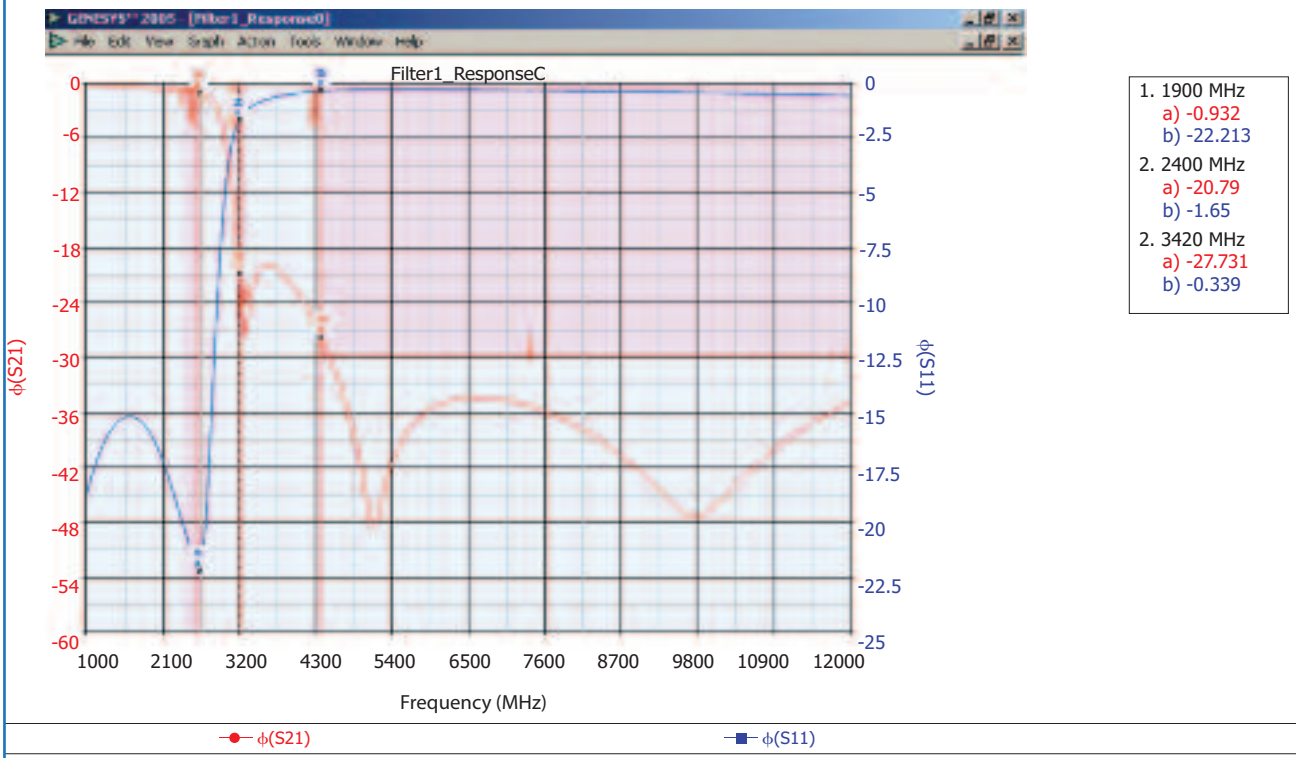
Lumped - Element Topology



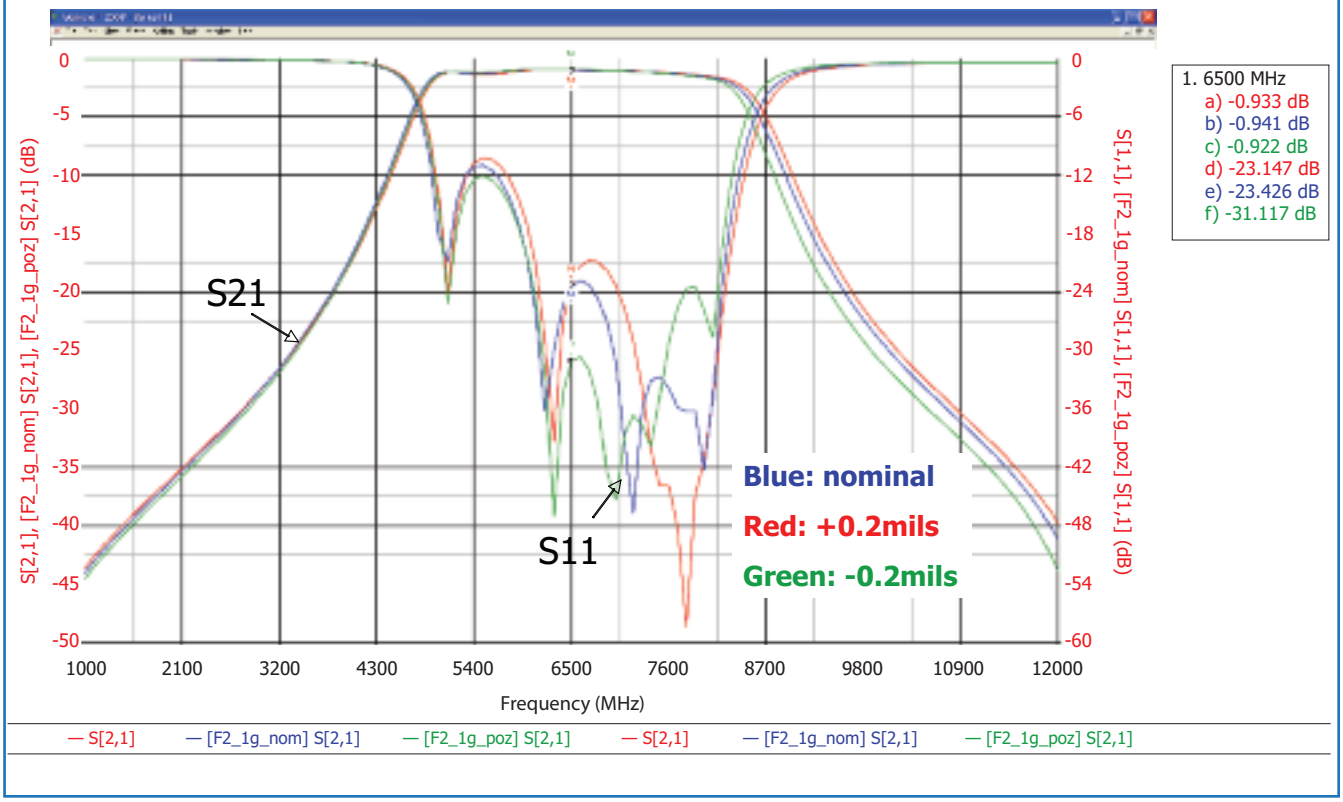
Distributed Band-Pass Topology



HFSS Simulation Lumped-Element Topology



S-Parameters as Simulated by HFSS (Process line-width sensitivity)



Assemblies

ATC // AVX assembly begins with high-precision pick-and-place of surface mount devices 0201 and larger including CSPs, µBGAs, flip-chips, ultra-fine-pitch [.012" (0.3 mm) lead pitch] QFPs and irregularly shaped components requiring ± .0005" (± .0125 mm) placement accuracy.

Die attach includes:

- Adhesive die attach – electrically / thermally conductive or electrically insulating epoxies
- Solder Die attach – lead or lead free for example, Sn63/Pb, 95Pb-5Sn,80Au-20Sn,88Pb,SAC305
- Wire/Ribbon Bonding – automated ball and wedge bonding, ribbon / wedge bonding and gold stud bumping.

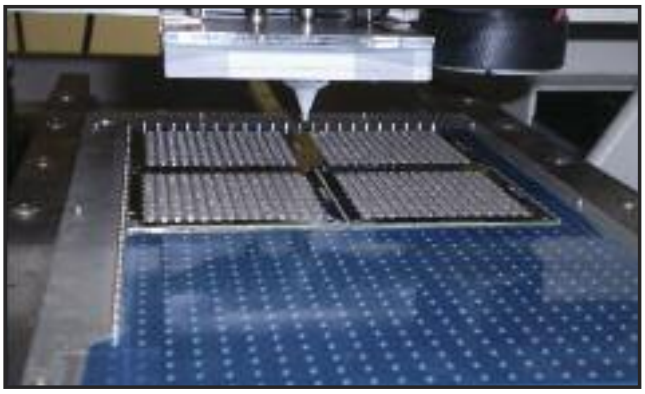
Encapsulation:

- Includes polymers, hermetic and non-hermetic structures and in-house fabricated ceramic enclosures.

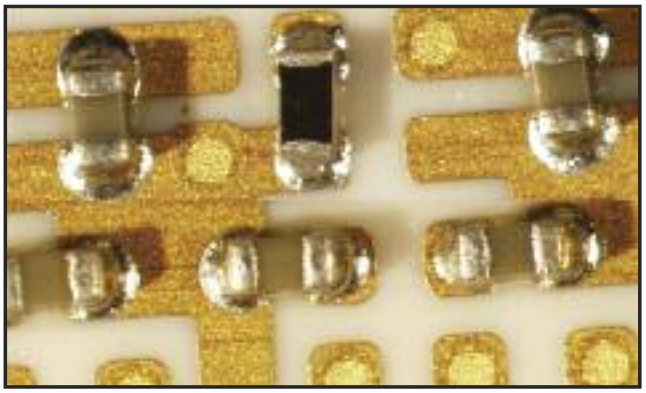
Additional assembly processes:

- Screen and stencil printing
- Automated dispensing (>7 mil diameter dots and lines)
- Parallel gap welding
- Solder tinning
- Via plugging (gold paste/epoxies)
- Solder mask application

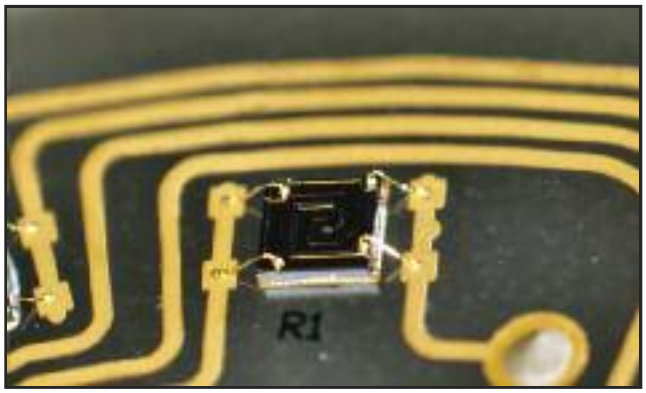
Pick and Place



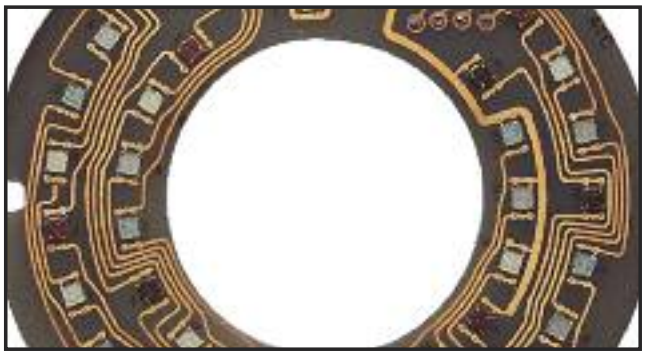
Capacity 13,000 Chips per Hour



0201 Soldered to Filled Vias



Epoxy LED Attachment and Wire Bonding



Two-sided assembly (top)

Two-sided assembly (bottom)

Inspection Methods

Visual	100%	Per MIL-STD-883, method 2032 Class H or K (10X microscope min.); IPC-A-610
Dimensional	AQL	Pattern features: Microscope; Substrate: Micrometer and calipers
Resistors	AQL	2 or 4 Point Probe
Adhesion	AQL	Tape pull test with 3M #610 tape
Other	Customer Specified	

General Ordering Information

Substrates	Type, surface finish, dimensions and tolerances.
Resistsive Films	Type, nominal resistivity, tolerance after heat treatment. Heat treatment temperature and time.
Conductive Films	Type, thickness and tolerance.
General	Specifications and acceptance criteria.
Artwork	Dimensioned Drawings, DXF, DWG, Gerber or GDS Formats.
Processing	Temperatures, bonding/soldering methods and environment.

Contact Information

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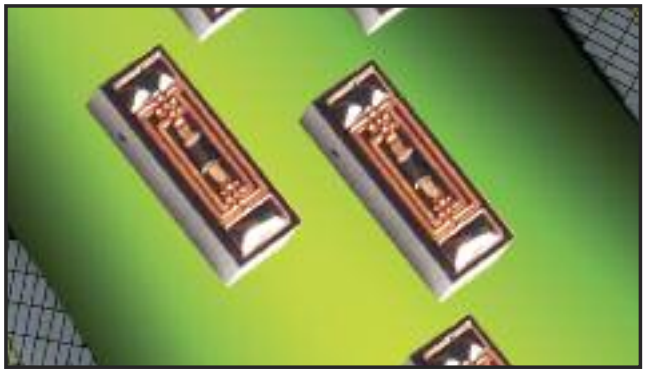
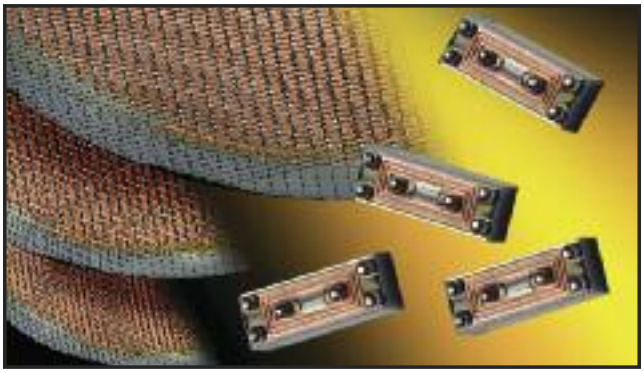


LGA 0402 Filters



BGA 0603 Filters

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